What is claimed is:

1. A semiconductor substrate having an element isolation region formed at the upper surface of a semiconductor substrate and a device region sandwiched by the element isolation region, the element isolation region comprising:

(a) a plurality of grooves formed in the semiconductor substrate; and

(b) buried oxide films formed in the grooves, the buried oxide films being formed by any of organic silicon based CVD method, spin-on-glass coating method, and anodic oxidation method and being composed of an oxide film which is annealed at a temperature of 1100 to 1350 ℃ .

2. The substrate of claim 1, wherein an aspect ratio d/l_1 , which is defined by a dimensional ratio of a depth d of the grooves to a width l_1 of openings of the grooves is less than 10.

3. The substrate of claim 2, wherein a repetitive pattern having a line-and-space ratio l_1/l_2 , which is defined as a ratio of a minimum space width l_1 corresponding to a width of openings of the grooves to a minimum line width l_2 corresponding to a width of the device region, of less than 1.5 are formed along a specified direction at a surface of the semiconductor substrate.

4. A semiconductor substrate having an element isolation region formed at the upper surface of a semiconductor substrate and a device region sandwiched by the element isolation region, the element isolation region comprising:

(a) grooves formed in the semiconductor substrate; and

(b) buried oxidation films formed in the grooves, the buried oxidation films being formed of the non-crystalline silicon oxide film which includes higher order ring structures of more than 5-fold ring and lower order ring

structures of less than 4-fold ring at respective predetermined rates.

5. The substrate of claim 4, wherein the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that the higher order ring structures of more than 5-fold ring are substantially more than 85 % of an overall structure and the lower order ring structures of less than 4-fold ring are substantially less than 15 % of the overall structure.

6. The substrate of claim 4, wherein the buried oxidation films are formed by any of organic silicon based CVD method, spin-on-glass coating method, and anodic oxidation method, and are composed of an oxide film which is annealed at a temperature of 1100 to 1350 °C.

7. The substrate of claim 4, wherein an aspect ratio d/l_1 which is defined by a dimensional ratio of a depth d of the grooves to a width l_1 of openings of the grooves is less than 10.

8. The substrate of claim 4, wherein a repetitive pattern having a line-and-space ratio l_1/l_2, which is defined as a ratio of a minimum space width l1 corresponding to a width of openings of the grooves to a minimum line width l_2 corresponding to a width of the device region, of less than 1.5 are formed along a specified direction at a surface of the semiconductor substrate.

9. A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) a first step of forming a plurality of grooves on

part of a surface of the semiconductor substrate;

(b) a second step of burying oxide films in the grooves by an organic silicon based CVD method; and

(c) a third step of annealing the oxide films at a substrate temperature of 1100 to 1350 ℃ .

10. The method of claim 9, wherein the organic silicon based CVD method in the second step is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

11. The method of claim 9, wherein the annealing in the third step is carried out in any one of reductive gas such as H_2 , inert gas such as He, Ne, Ar, Kr, or Xe, O_2 , N_2 , HCl, CO, and CO_2 , or in a gas mixture consisting of any mixture of two kinds of gas selected from these gases.

12. The method of claim 9, wherein the second step deposits an oxide film thicker than a depth of the grooves and then planarizes a surface of a resultant structure until a surface of the semiconductor substrate is substantially exposed.

13. The method of claim 9, wherein the second step is a step of depositing an oxide film thicker than a depth of the grooves, and further comprising, after the third step, a fourth step of planarizing a surface of a resultant structure until a surface of the semiconductor substrate is substantially exposed.

14. The method of claim 9, wherein the first step is a step of forming the grooves having an aspect ratio d/l_1 of less than 10, which is defined by a dimensional ratio of a depth d to a width l_1 of openings.

15. The method of claim 9, wherein the first step is a

step of forming the grooves as cyclic line and space patterns having a line-and-space ratio l_1/l_2, which is defined as a ratio of minimum space width l_1 corresponding to a width of openings of the grooves to a minimum line width l_2 corresponding to a width of a region sandwiched by the groove, of less than 1.5, along a specified direction.

16. A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) a first step of forming a silicon direct bonding oxide film on a first principal surface of a first semiconductor substrate in terms of an organic silicon based CVD method, then carrying out first annealing at a substrate temperature of 1100 to 1350 ℃, and then planarizing a surface of the silicon direct bonding oxide film formed on the first principal surface of the first semiconductor substrate, otherwise a first step of forming a silicon direct bonding oxide film on a first principal surface of a first semiconductor substrate in terms of an organic silicon based CVD method, then planarizing a surface of the silicon direct bonding oxide film formed on the first principal surface of the first semiconductor substrate, and then carrying out first annealing at a substrate temperature of 1100 to 1350 ℃;

(b) a second step of directly bonding the first semiconductor substrate to a second semiconductor substrate being different from the first semiconductor substrate via the silicon direct bonding oxide film and then adjusting the first semiconductor substrate to a predetermined thickness;

(c) a third step forming a plurality of grooves at part of a second principal surface of the first semiconductor substrate which is located on a side not to mate with the second semiconductor substrate;

(d) a fourth step of forming buried oxide films in the grooves formed by the third step by the organic silicon

based CVD method; and

(e) a fifth step of carrying out second annealing of the buried oxide films at a substrate temperature of 1100 to 1350 ℃ .

17. The method of claim 16, wherein the organic silicon based CVD method in the first and fourth steps is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

18. The method of claim 16, wherein the first and second annealing is carried out in any one of reductive gas such as H_2 , inert gas such as He, Ne, Ar, Kr, or Xe, O_2 , N_2 , HCl, CO, and CO_2 , or in a gas mixture consisting of any mixture of two kinds of gas selected from these gases.

19. The method of claim 16, wherein the fourth step deposits an oxide film thicker than a depth of the grooves and then planarizes a surface of a resultant structure until the second principal surface of the first semiconductor substrate is substantially exposed.

20. The method of claim 16, wherein the fourth step is a step of depositing an oxide film thicker than a depth of the grooves, and further comprising, after the fifth step, a sixth step of planarizing a surface of a resultant structure until the second principal surface of the first semiconductor substrate is substantially exposed.

21. The method of claim 16, wherein the third step is a step of forming the grooves having an aspect ratio d/l_1 of less than 10, which is defined by a dimensional ratio of a depth d to a width l_1 of openings.

22. The method of claim 16, wherein the third step is a

step of forming the grooves as cyclic line and space patterns, the grooves having the width l_1 of openings of the grooves giving a minimum space width and a width l_2 of the device region giving a minimum line width, and a ratio l_1/l_2 measured along a specified direction is less than 1.5.

23. A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) a first step of forming a plurality of grooves on part of a first principal surface of a first semiconductor substrate;

(b) a second step of forming a silicon direct bonding oxide film on the first principal surface of the first semiconductor substrate by an organic silicon based CVD method, then carrying out annealing of a resultant structure at a substrate temperature of 1100 to 1350 ℃, and then planarizing a surface of the silicon direct bonding oxide film formed on the first principal surface of the first semiconductor substrate, otherwise a second step of forming a silicon direct bonding oxide film on the first principal surface of the first semiconductor substrate in terms of an organic silicon based CVD method, then planarizing a surface of the silicon direct bonding oxide film formed on the first principal surface of the first semiconductor substrate, and then carrying out annealing at a substrate temperature of 1100 to 1350 ℃ ; and

(c) a third step of directly bonding the first semiconductor substrate to a second semiconductor substrate being different from the first semiconductor substrate via the silicon direct bonding oxide film and then thinning a thickness of the first semiconductor substrate until part of the silicon direct bonding oxide film is exposed to form device regions sandwiched by the silicon direct bonding oxide film.

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